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ART UNIT	**PAPER NUMBER**
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/876,290	YANAGISAWA ET AL.	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,11-15 and 20* is/are pending in the application.

4a) Of the above claim(s) *3-6,12,13 and 15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7,11,14 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2-28-7,9-13-6,8-23-5,12-13-4,6-7-1* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following features must be shown or the feature(s) canceled from the claim(s):

Re claim 1: so as to rigidly restrict displacement of said semiconductor modules.

Re claim 2: two pairs of opposing side walls.

Re claim 11: so as to rigidly restrict displacement of said semiconductor modules.

Re claim 14: two pairs of substantially parallel opposed side walls; so as to rigidly restrict displacement of said semiconductor modules; said two pairs of opposed side walls.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 2, 7, 11, 14 and 20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The undescribed subject matter is the following:

Re claim 1: so as to rigidly restrict displacement of said semiconductor modules.

Re claim 2: two pairs of opposing side walls.

Re claim 11: so as to rigidly restrict displacement of said semiconductor modules.

Re claim 14: two pairs of substantially parallel opposed side walls; so as to rigidly restrict displacement of said semiconductor modules; said two pairs of opposed side walls.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 2, 7, 11 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

There is insufficient antecedent basis for the following claim language:

Re claim 1: said base member (both occurrences).

Re claim 11: said base member (both occurrences).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 7, 11 and 14 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Normington (5397916).

At column 3, line 58 to column 10, line 47, Normington discloses the following:

Re claim 1: A multilayer semiconductor device assembly jig for securing a plurality of semiconductor modules disposed within the assembly jig comprising: a lateral position restriction structure “sides”/131, 132/231, 232 for maintaining alignment of a plurality of stacked semiconductor modules “subassemblies” with their respective lateral positions mutually restricted, the lateral position restriction structure formed at a width slightly more than but substantially equal to a width of a rigid “adequate stiffness” portion 21, 23, 24 “the lead and polyimide layer provides adequate stiffness [rigidness] along the edge of the die” of said plurality of semiconductor modules so as to inherently rigidly restrict displacement of said semiconductor modules; a removable height

restriction mechanism 91/133/252 disposed opposite said base member and which interfaces with said lateral position restriction structure for restricting an entire height of said semiconductor modules layered on said base member; the jig having a mother substrate 91/133/252/"printed circuit board" alignment structure 92/253 for securing the mother substrate to the jig; and wherein each of the plurality of semiconductor modules secured within the jig is comprised of one or more semiconductor chips 21 secured to a printed wiring board 51 that has electrical connections 24 on a top and bottom surface thereof and wherein adjacent semiconductor modules are secured to one another by solder connections "solder glass" "Die 203 is attached to separator by conductive epoxy, eutectic bonding, solder or glass" between respective top and bottom surfaces thereof.

Re claim 2: The multilayer semiconductor device assembly jig according to claim 1, wherein said lateral position restriction structure comprises a substantially rectangular-shaped structure comprising two pairs of opposing side walls "sides"/131, 132 and which is positioned on said base member and which has a storage space for storing said semiconductor modules in a layered state, wherein an inner wall surface of said storage space constitutes said lateral position restriction structure.

Re claim 7: The multilayer semiconductor device assembly jig according to claim 1, wherein said height restriction mechanism comprises: a cover member 91/133/252 secured over or on said lateral position restriction structure

Re claim 11: A multilayer semiconductor device assembly jig for securing a plurality of semiconductor modules disposed within the assembly jig comprising: a

lateral position restriction structure for maintaining alignment of a plurality of stacked semiconductor modules with their respective lateral positions mutually restricted, the lateral position restriction structure comprised of at least two opposed side walls having a single stack of the semiconductor modules therebetween, the sidewalls being formed at a width slightly more than but substantially equal to a width of a rigid portion of said plurality of semiconductor modules so as to rigidly restrict displacement of said semiconductor modules; a removable height restriction mechanism disposed opposite said base member and which interfaces with said lateral position restriction structure for restricting an entire height of said semiconductor modules layered on said base member; a mother substrate alignment structure secured to the jig; and further wherein each of the plurality of semiconductor modules secured within the jig is comprised of one or more semiconductor chips secured to a printed wiring board that has electrical connections on a top and bottom surface thereof and wherein adjacent semiconductor modules are secured to one another by solder connections between respective top and bottom surfaces thereof.

Re claim 14: An assembly jig for securing a plurality of semiconductor modules disposed within the assembly jig comprising: two pairs of substantially parallel opposed side walls secured to a solid base member, the sidewalls being formed at a width slightly more than but substantially equal to a width of a rigid portion of said plurality of semiconductor modules so as to rigidly restrict displacement of said semiconductor modules; a removable cover member located opposite said base member and which interfaces with the side walls; an internal void defined by said two pairs of opposed side

walls providing a reception area for a plurality of semiconductor modules such that modules disposed within the void are aligned and their lateral motion (at least their lateral motion beyond the side walls) is prevented by the side wails, and wherein the semiconductor modules are comprised of at least one chip and one wiring board; and further wherein the removable cover member is positioned such that it prevents vertical displacement of an uppermost semiconductor module.

The following is further clarified:

Re claim 1: so as to inherently rigidly restrict displacement of said semiconductor modules.

Specifically, the lateral position restriction structure rigidly restricts displacement of the module at least via the “adequate stiffness” portion 21, 23, 24. In addition, the lateral position restriction structure rigidly restricts displacement of the module at least because the displacement of the outer shape 21, 13, 24 of the module is maintained by the fixed lateral position framework.

The following is further clarified:

Re claim 2: two pairs of opposing side walls 131, 132.

Specifically, as cited, Normington discloses, “The sides do not fill the available space between the corners of perimeter frame 134. This provides a gap, such as gap 137, at each corner of the package." In addition, in FIG. 9, Normington illustrates four package corners. Therefore, in order for the sides (side walls) to provide a gap at each of the four corners, there must be at least four (two pairs of) sides.

In any case, the following language is statements of intended use of the claimed jig apparatus:

Re claim 1: multilayer semiconductor device assembly [i.e., for multilayer semiconductor device assembly]; for securing a plurality of semiconductor modules disposed within the assembly jig; lateral position restriction [i.e., for lateral position restriction]; for maintaining alignment of a plurality of stacked semiconductor modules with their respective lateral positions mutually restricted; so as to rigidly restrict displacement of said semiconductor modules; removable [i.e., for being removed]; height restriction [i.e., for height restriction]; for restricting an entire height of said semiconductor modules layered on said base member; mother substrate alignment [i.e., for mother substrate alignment]; for securing the mother substrate to the jig.

Re claim 2: storage [i.e., for storage]; for storing said semiconductor modules in a layered state.

Re claim 7: cover [i.e., for cover].

Re claim 11: multilayer semiconductor device assembly [i.e., for multilayer semiconductor device assembly]; for securing a plurality of semiconductor modules disposed within the assembly jig; lateral position restriction [i.e., for lateral position restriction]; for maintaining alignment of a plurality of stacked semiconductor modules with their respective lateral positions mutually restricted; so as to rigidly restrict displacement of said semiconductor modules; removable [i.e., for being removed]; height restriction [i.e., for height restriction]; for restricting an entire height of said

semiconductor modules layered on said base member; mother substrate alignment [i.e., for mother substrate alignment].

Re claim 14: assembly [i.e., for assembly]; for securing a plurality of semiconductor modules disposed within the assembly jig; so as to rigidly restrict displacement of said semiconductor modules; removable [i.e., for being removed]; cover [i.e., for cover]; reception [i.e., for reception] for a plurality of semiconductor modules such that modules disposed within the void are aligned and their lateral motion is prevented by the side wails, and wherein the semiconductor modules are comprised of at least one chip and one wiring board; such that it prevents vertical displacement of an uppermost semiconductor module.

Moreover, the statements of intended use do not appear to result in a structural difference between the claimed apparatus and the apparatus of Normington.

To this end, the resulting structure of the claimed apparatus apparently identical to the structure of the apparatus of Normington is the following:

Re claim 1: A jig; a structure; the structure formed at a width slightly more than but substantially equal to a width of a rigid portion of said plurality of semiconductor modules; a mechanism disposed opposite said base member and which interfaces with said structure; the jig having a structure; and wherein each of the plurality of semiconductor modules secured within the jig is comprised of one or more semiconductor chips secured to a printed wiring board that has electrical connections on a top and bottom surface thereof and wherein adjacent semiconductor modules are

secured to one another by solder connections between respective top and bottom surfaces thereof.

Re claim 2: The jig according to claim 1, wherein said structure comprises a substantially rectangular-shaped structure comprising two pairs of opposing side walls and which is positioned on said base member and which has a space; wherein an inner wall surface of said space constitutes said structure.

Re claim 7: The jig according to claim 1, wherein said mechanism comprises: a member secured over or on said structure

Re claim 11: A jig comprising: a structure; the structure comprised of at least two opposed side walls having a single stack of the semiconductor modules therebetween, the sidewalls being formed at a width slightly more than but substantially equal to a width of a rigid portion of said plurality of semiconductor modules; a mechanism disposed opposite said base member and which interfaces with said structure; a structure secured to the jig; wherein each of the plurality of semiconductor modules secured within the jig is comprised of one or more semiconductor chips secured to a printed wiring board that has electrical connections on a top and bottom surface thereof and wherein adjacent semiconductor modules are secured to one another by solder connections between respective top and bottom surfaces thereof.

Re claim 14: A jig comprising: two pairs of substantially parallel opposed side walls secured to a solid base member, the sidewalls being formed at a width slightly more than but substantially equal to a width of a rigid portion of said plurality of semiconductor modules; a removable member located opposite said base member and

which interfaces with the side walls; an internal void defined by said two pairs of opposed side walls providing an area; such that modules disposed within the void are aligned and their lateral motion is prevented by the side wails, and wherein the semiconductor modules are comprised of at least one chip and one wiring board; member is positioned.

Further, because the apparatus of Normington appears to have the same structure as the claimed apparatus, it appears to be capable of being used for the intended uses, and the statements of intended use do not patentably distinguish the claimed apparatus from the apparatus of Normington. The manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

Furthermore, it is noted that, "Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)); and, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex

parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). Therefore, the following materials or articles worked upon by the claimed jig structure do not impart patentability to, and are of no significance in determining patentability of, the jig apparatus claims:

Re claim 1: each of the plurality of semiconductor modules secured within the jig is comprised of one or more semiconductor chips secured to a printed wiring board that has electrical connections on a top and bottom surface thereof and wherein adjacent semiconductor modules are secured to one another by solder connections between respective top and bottom surfaces thereof.

Re claim 11: each of the plurality of semiconductor modules secured within the jig is comprised of one or more semiconductor chips secured to a printed wiring board that has electrical connections on a top and bottom surface thereof and wherein adjacent semiconductor modules are secured to one another by solder connections between respective top and bottom surfaces thereof.

Re claim 14: modules disposed within the void are aligned and their lateral motion is prevented by the side wails, and wherein the semiconductor modules are comprised of at least one chip and one wiring board; an uppermost semiconductor module.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

In the alternative, claims 1, 2, 7, 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Normington (5397916).

Normington is applied as it is applied to claims 1, 2, 7, 11 and 14 supra.

However, Normington does not appear to disclose verbatim the particular claimed width.

Notwithstanding, as reasoned from well established legal precedent, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose this particular dimension because applicant has not disclosed that, in view of the applied prior art, the dimension is for a particular **unobvious** purpose, produces an unexpected result, or is otherwise critical. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular **unobvious** purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531

F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Moreover, it would have been obvious to try the particular claimed width because this would have been a known option within the technical grasp of a person of ordinary skill in the art that would lead to anticipated success and, "a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense." KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (U.S. 2007). See also, Pfizer Inc. v. Apotex Inc., 82 USPQ2d 1852 (Fed. Cir. 2007). Merck & Co., Inc. v. Biocraft Labs., Inc., 874 F.2d 804, 807 (Fed. Cir. 1989). Ex parte Min-Hong Fu, Colleen A. Helbig, Kent J. Evans, Kathleen M. Carmichael, and David M. Skinner, Appeal 2008-0601, 03-31-2008.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Normington as applied to claim 1, and further in combination with Woodman (5016138).

Normington does not appear to explicitly disclose the following:

Re claim 20: The multilayer semiconductor device assembly jig according to claim 1, wherein said mother substrate alignment structure is formed in said lateral position restriction mechanism as a hole that receives a pin member.

Regardless, at column 6, lines 6-24; and column 7, lines 18-27, Woodman discloses wherein a mother substrate alignment structure 54 is formed in a lateral position restriction mechanism 50 as a hole 54 that receives a pin member 26/90.

In addition, it would have been obvious to combine this disclosure of Woodman with the disclosure of Normington because it would facilitate physical and electrical connection of the mechanism of Normington.

In any case, the following language is a statement of intended use of the claimed jig apparatus:

Re claim 20: that receives a pin member.

Moreover, the statement of intended use does not appear to result in a structural difference between the claimed apparatus and the apparatus of the combination of Normington and Woodman.

To this end, the resulting structure of the claimed apparatus apparently identical to the structure of the apparatus of the combination of Normington and Woodman is the following:

Re claim 20: The jig according to claim 1, wherein said structure is formed in said mechanism as a hole.

Further, because the apparatus of Normington appears to have the same structure as the claimed apparatus, it appears to be capable of being used for the intended use, and the statement of intended use does not patentably distinguish the claimed apparatus from the apparatus of Normington.

Applicant's amendment and remarks filed 4-25-8 have been fully considered, are treated supra and infra, or have been previously addressed in the record.

Applicant argues:

> The remaining pair of opposed sidewalls is not shown in these illustrations because, as described in the specification, the box shaped structure would of course include the

> remaining pair of opposed sidewalls, but this portion has been cutaway from the illustration so that the internal portion of the assembly jig can be readily viewed. Applicants respectfully submit that no drawing modification is required in light of the foregoing explanation. There should be no doubt that a person of ordinary skill the art [sic] with even the most basic understanding of engineering drawings having the specification in hand would readily understand that the illustration of the box-shaped structure as noted would include an additional pair of opposed sidewalls which are not shown because this are [sic], of course cutaway side view illustrations.

It is respectfully noted that applicant's statement, "The remaining pair of opposed sidewalls is not shown in these illustrations," is an admission that the following features are not shown in the drawings:

Re claim 2: two pairs of opposing side walls.

Re claim 14: two pairs of substantially parallel opposed side walls; said two pairs of opposed side walls.

The argument is further respectfully traversed because applicant merely cites "the specification" without elucidation; and the citation to "the specification" does not otherwise appear to support the argument.

Furthermore, it is respectfully suggested that a person of ordinary skill in the art with even the most basic understanding of engineering drawings having the specification in hand would not readily understand that the illustration of the alleged box-shaped structure as noted would include an additional pair of opposed sidewalls which are not shown because these are, of course, cutaway side view illustrations. To further clarify, the disputed cutaway portion that applicant admits is not shown in the drawings is not necessarily a pair of opposed sidewalls. For example, the disputed, non-illustrated cutaway portion could merely be an identical extension of the illustrated cutaway portion. To this end, Lutzenberger, at column 3, lines 7-9, evidences an

analogous cutaway portion in FIG. 2 [looking in the opposite direction of the arrows] which is a substantially identical extension of the cutaway portion of FIG. 2A.

Also, applicant alleges:

> This structure could not possibly be considered an assembly jig because the sidewalls of the structure actually provide the electrical communication and cannot be withdrawn as an assembly jig would normally be removed.

This allegation is respectfully traversed because a disclosure in Normington that the sidewalls of the structure actually provide the electrical communication would not necessarily be mutually exclusive with the disclosure of an assembly jig.

Moreover, it is respectfully submitted that the assertion, “and cannot be withdrawn as an assembly jig would normally be removed” is unsupported by proof or a showing of facts; hence, it essentially amounts to mere conjecture and it is of no probative value. See MPEP 716.01(c), and, Ex parte Gray, 10 USPQ2d 1922 (Bd. Pat. App. & Inter. 1989) (statement in publication dismissing the "preliminary identification of a human b - NGF - like molecule" in the prior art, even if considered to be an expert opinion, was inadequate to overcome the rejection based on that prior art because there was no factual evidence supporting the statement); In re Beattie, 974 F.2d 1309, 24 USPQ2d 1040 (Fed. Cir. 1992) (declarations of seven persons skilled in the art offering opinion evidence praising the merits of the claimed invention were found to have little value because of a lack of factual support); Ex parte George, 21 USPQ2d 1058 (Bd. Pat. App. & Inter. 1991) (conclusory statements that results were "unexpected," unsupported by objective factual evidence, were considered but were not found to be of substantial evidentiary value).

In any case, the scope of the claims is not necessarily limited to an intended use of the jig apparatus wherein the sidewalls can be withdrawn allegedly as an assembly jig would normally be removed; and Normington is not necessarily applied for this disclosure.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions relevant to the examination of the instant invention.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

For information on the status of this application applicant should check PAIR:
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

/David E Graybill/
Primary Examiner, Art Unit 2822